Applicant(s)	Jack Linn et al.
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Group Art Unit	2829
Examiner Name	Ashok K. Sarkar
Attorney Docket No.	125.013US02

AMENDMENT AND RESPONSE UNDER 37 C.F.R. §1.111

Title: BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC GETTERING ZONE (as amended)

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on May 20, 2002. In response to the Office action, please consider the following:

IN THE TITLE

Please amend the title as follows:

C1 "BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANAR INTRINSIC GETTERING ZONE"

IN THE CLAIMS

Please amend Claims 24, 26, 28, 30, 38, 39, 40 and 46 as follows:

24. (Amended Twice) A semiconductor device formed by the method comprising:

providing a wafer comprising a monocrystalline semiconductor material;

C7 implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged